

WHAT IS CLAIMED IS:

1. A circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment, comprising:

5 a memory for temporarily accumulating a low-order group signal,

a multiplexing circuit for multiplexing an output signal output by said memory with an overhead bit necessary for optical digital transmission, and

10 a pattern generation circuit for generating an unfixed pattern having no fixed value and outputting the pattern to said multiplexing circuit.

2. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 1, wherein

5 said unfixed pattern is applied to said multiplexing circuit while said memory outputs a fixed pattern.

3. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 1, further comprising

5 a selection circuit connected between said multiplexing circuit and said memory, wherein

between said fixed pattern output by said memory

and said unfixed pattern output by said pattern generation circuit, said selection circuit selects said unfixed pattern.

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4. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 3, further comprising a phase comparator for outputting a reset signal

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which resets said memory based on a phase difference between a phase of write to said memory and a phase of read from the memory, wherein

said selection circuit selects said unfixed pattern based on said reset signal.

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5. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 3, further comprising

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difference between a phase of write to said memory and a phase of read from the memory and when said phase difference is larger than a set value set in advance, outputting a reset signal which resets said memory, wherein

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said selection circuit selects said unfixed pattern based on said reset signal.

6. The circuit for preventing transmission of a

fixed pattern of an optical digital transmission equipment according to claim 4, further comprising a reset signal detection circuit for outputting a switching signal based on a read address signal applied to said memory from when said memory is reset until when a signal first written into said memory is read from said memory, wherein

10 said selection circuit selects said unfixed pattern based on said reset signal and said switching signal.

7. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 4, further comprising

a reset signal detection circuit for detecting  
said reset signal, wherein

a read address signal applied to said memory is also applied to said reset signal detection circuit,

said reset signal detection circuit outputs a  
switching signal based on said read address signal from

when said memory is reset until when a signal first written into said memory is read from said memory, and

said selection circuit selects said unfixed pattern based on said reset signal and said switching signal.

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8. The circuit for preventing transmission of a

fixed pattern of an optical digital transmission equipment according to claim 6, further comprising  
a determination circuit and an OR circuit,  
5 wherein

said determination circuit is provided between said OR circuit and an input side of said memory,

said determination circuit outputs a switch signal when a signal written into said memory has a fixed pattern for a set time,  
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to said OR circuit, said switching signal and said switch signal are applied, and

said selection circuit selects said unfixed pattern based on said switch signal in addition to said reset signal and said switching signal.  
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9. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 1, wherein  
said unfixed pattern is a random pattern.

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10. A circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment, comprising:

a memory for temporarily storing data,

5 a multiplexing circuit for multiplexing a signal output by said memory with an overhead bit necessary for optical digital transmission,

10                   a pattern generation circuit for generating an  
unfixed pattern having no fixed value and outputting the  
pattern to said multiplexing circuit,

an E/O conversion unit for converting a signal  
output by said multiplexing circuit into an optical  
signal,

15                   an optical fiber for transmitting an optical  
signal output by said E/O conversion unit, and

an O/E conversion unit for converting an optical  
signal output by said optical fiber into an electric  
signal, wherein

20                   while said memory outputs a fixed pattern, the  
unfixed pattern is applied to said multiplexing circuit.

11.                 The circuit for preventing transmission of a  
fixed pattern of an optical digital transmission  
equipment according to claim 10, wherein  
said unfixed pattern is a random pattern.

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12.                 The circuit for preventing transmission of a  
fixed pattern of an optical digital transmission  
equipment according to claim 10, further comprising  
a selection circuit connected between said  
multiplexing circuit and said memory, wherein  
between said fixed pattern output by said memory  
and said unfixed pattern output by said pattern  
generation circuit, said selection circuit selects said

unfixed pattern.

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13. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 12, further comprising

a phase comparator for outputting a reset signal

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which resets said memory based on a phase difference between a phase of write to said memory and a phase of read from the memory, wherein

said selection circuit selects said unfixed pattern based on said reset signal.

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14. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 12, further comprising

a phase comparator for comparing a phase

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difference between a phase of write to said memory and a phase of read from the memory and when said phase difference is larger than a set value set in advance, outputting a reset signal which resets said memory, wherein

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said selection circuit selects said unfixed pattern based on said reset signal.

15. The circuit for preventing transmission of a fixed pattern of an optical digital transmission equipment according to claim 13, further comprising

5 a reset signal detection circuit for outputting a  
switching signal based on a read address signal applied  
to said memory from when said memory is reset until when  
a signal first written into said memory is read from  
said memory, wherein

10 said selection circuit selects said unfixed  
pattern based on said reset signal and said switching  
signal.

16. The circuit for preventing transmission of a  
fixed pattern of an optical digital transmission  
equipment according to claim 13, further comprising  
a reset signal detection circuit for detecting

5 said reset signal, wherein

a read address signal applied to said memory is  
also applied to said reset signal detection circuit,

10 said reset signal detection circuit outputs a  
switching signal based on said read address signal from  
when said memory is reset until when a signal first  
written into said memory is read from said memory, and

said selection circuit selects said unfixed  
pattern based on said reset signal and said switching  
signal.

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17. The circuit for preventing transmission of a  
fixed pattern of an optical digital transmission  
equipment according to claim 15, further comprising

a determination circuit and an OR circuit,

## 5           wherein

~~said determination circuit is provided between  
said OR circuit and an input side of said memory,~~

10        said determination circuit outputs a switch signal when a signal written into said memory has a fixed pattern for a set time,

to said OR circuit, said switching signal and  
said switch signal are applied, and

15       said selection circuit selects said unfixed  
pattern based on said switch signal in addition to said  
reset signal and said switching signal.